WHAT IS CLAIMED IS:

1. A method for fabricating a low temperature polysilicon thin film transistor, comprising the steps of:

providing a substrate ;

forming a buffer layer over the substrate ;

forming a low surface energy material layer over the buffer layer ;

forming a first amorphous silicon layer over the low surface energy material layer;

melting the first amorphous silicon layer by a laser annealing step to transform the liquid first amorphous silicon layer into a plurality of polysilicon seeds uniformly distributed on the low surface energy material layer;

forming a second amorphous silicon layer over the low surface energy material layer and covering the polysilicon seeds; and

melting the second amorphous silicon layer by the laser annealing step to crystallize the liquid second amorphous silicon layer into a polysilicon layer with the associated polysilicon seeds.

2. The method according to claim 1, wherein the thickness of the second amorphous silicon layer is larger than the thickness of the first amorphous silicon layer.

3. The method according to claim 2, wherein the thickness of the first amorphous silicon layer is preferably 50 angstrom (Å).

4. The method according to claim 3, wherein the thickness of the second amorphous silicon layer is preferably about 450 Å.

5. The method according to claim 1, wherein the substrate is a glass substrate.

6. The method according to claim 1, wherein the buffer layer is a silicon dioxide layer.

7. The method according to claim 1, wherein the method further comprises the steps of:

eliminating portions of the polysilicon layer to form a polysilicon island;

doping both ends of the polysilicon island where to respectively form a heavily doped n type (n+) ohmic contact layer, which is also respectively in contact with a residual polysilicon island;

forming a first insulating layer over the n+ ohmic contact layer, the residual polysilicon island, and portions of the low surface energy material layer;

doping both ends of the residual polysilicon island to form a lightly doped n type (n-) ohmic contact layer and a polysilicon channel area, wherein the n- ohmic contact layer is respectively located between the polysilicon channel area and the n+ ohmic contact layers;

forming a gate, which is disposed at a location opposite to the polysilicon channel area, on the first insulating layer;

forming a second insulating layer on the first insulating layer to cover the gate, wherein there are a first contact hole and a second contact hole penetrating through both of the second insulating layer and the first insulating layer, and the first contact hole as well as the second contact hole are selectively located near the lateral ends of the gate to expose the n+ ohmic contact layers;

forming a source and a drain within the first contact hole and the second contact hole respectively and on the portions of the second insulating layer, wherein the source and the drain are electrically connected to the n+ ohmic contact layers via the first contact hole and the second contact hole,

respectively;

forming a passivation layer on the second insulating layer, the source, and the drain, wherein the passivation layer comprises a third contact hole for exposing portions of the source or the drain; and

forming an indium tin oxide (ITO) electrode on the passivation and within the third contact hole, so that the ITO electrode is electrically connected to the source or the drain via the third contact hole.

8. A method for fabricating a low temperature polysilicon thin film transistor, comprising the steps of:

providing a substrate ;

forming a buffer layer over the substrate ;

processing the surface of the buffer layer by a plasma hydrogenation step ;

forming a first amorphous silicon layer over the buffer layer;

melting the first amorphous silicon layer by a laser annealing step to transform the liquid first amorphous silicon layer into a plurality of polysilicon

seeds uniformly distributed on the buffer layer;

forming a second amorphous silicon layer over the buffer layer and covering the polysilicon seeds; and

melting the second amorphous silicon layer by the laser annealing step to crystallize the liquid second amorphous silicon layer into a polysilicon layer with the associated polysilicon seeds.

9. The method according to claim 8, wherein the second amorphous silicon layer is thicker than the first amorphous silicon layer.

10. The method according to claim 9, wherein the thickness of the first amorphous silicon layer is preferably about 50 Å.

11. The method according to claim 10, wherein thickness of the second amorphous silicon layer is preferably about 450 Å.

12. The method according to claim 8, wherein the substrate is a glass substrate.

13. The method according to claim 8, wherein the buffer layer is a silicon dioxide layer.

14. The method according to claim 8, wherein the method further comprises the steps of:

eliminating portions of the polysilicon layer to form a polysilicon island;

doping both ends of the polysilicon island where to respectively form a heavily doped n type (n+) ohmic contact layer, which is also respectively in contact with a residual polysilicon island;

forming a first insulating layer over the n+ ohmic contact layer, the residual polysilicon island, and portions of the buffer layer;

doping both ends of the residual polysilicon island to form a lightly doped n type (n-) ohmic contact layer and a polysilicon channel area, wherein the n- ohmic contact layer is respectively located between the polysilicon channel area and the n+ ohmic contact layers;

forming a gate, which is disposed at a location opposite to the polysilicon channel area, on the first insulating layer;

forming a second insulating layer on the first insulating layer to cover the gate, wherein a first contact hole and a second contact hole penetrate through both of the second insulating layer and the first insulating layer, and

selectively located near the lateral ends of the gate to expose the n+ ohmic contact layers;

forming a source and a drain disposed within the first contact hole and the second contact hole respectively and on the portions of the second insulating layer, wherein the source and the drain are electrically connected to the n+ ohmic contact layers via the first contact hole and the second contact hole, respectively;

forming a passivation layer on the second insulating layer, the source, and the drain, wherein the passivation layer comprises a third contact hole for exposing portions of the source or the drain; and

forming an indium tin oxide (ITO) electrode on the passivation and within the third contact hole such that the ITO electrode is electrically connected to the source or the drain via the third contact hole.

15. A method for fabricating a low temperature polysilicon thin film transistor, comprising the steps of:

providing a substrate ;

forming a silicon dioxide layer over the substrate ;

forming a low surface energy material layer over the silicon dioxide layer ;

forming a first amorphous silicon layer over the low surface energy material layer;

melting the first amorphous silicon layer by an laser annealing step to transform the liquid first amorphous silicon layer into a plurality of polysilicon seeds uniformly distributed on the low surface energy material layer;

forming a second amorphous silicon layer, which is thicker than the first amorphous silicon layer by the laser ancon layer, over the low surface energy material layer and covering the polysilicon seeds; and

melting the second amorphous silinealing step to crystallize the liquid second amorphous silicon layer into a polysilicon layer with the associated polysilicon seeds.

16. The method according to claim 15, wherein the thickness of the first amorphous silicon layer is preferably about 50 Å.

17. The method according to claim 16, wherein thickness of the second amorphous silicon layer is preferably about 450 Å.

18. The method according to claim 15, wherein the method further comprises the steps of:

eliminating portions of the polysilicon layer to form a polysilicon island;

doping both ends of the polysilicon island where to respectively form a heavily doped n type (n+) ohmic contact layer, which is also respectively in contact with a residual polysilicon island;

forming a first insulating layer over the n+ ohmic contact layer, the residual polysilicon island, and portions of the low surface energy material layer;

doping both ends of the residual polysilicon island to form a lightly doped n type (n-) ohmic contact layer and a polysilicon channel area, wherein the n- ohmic contact layer is respectively located between the polysilicon channel area and the n+ ohmic contact layers;

forming a gate, which is disposed at a location opposite to the polysilicon channel area, on the first insulating layer;

forming a second insulating layer on the first insulating layer to cover the gate , wherein there are a first contact hole and a the second contact hole

penetrating through both of the second insulating layer and the first insulating layer, and the first contact hole as well as the second contact hole are selectively located near the lateral ends of the gate to expose the n+ ohmic contact layers;

forming a source and a drain within the first contact hole and the second contact hole respectively and on the portions of the second insulating layer, wherein the source and the drain are electrically connected to the n+ ohmic contact layers via the first contact hole and the second contact hole, respectively;

forming a passivation layer on the second insulating layer, the source, and the drain, wherein the passivation layer comprises a third contact hole for exposing portions of the source or the drain; and

forming an indium tin oxide (ITO) electrode on the passivation and within the third contact hole, so that the ITO electrode is electrically connected to the source or the drain via the third contact hole.

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